REMARKS

Claims 8, 15, 23-41 are all the claims presently pending in the application. Claims 39-40 have been added to claim additional features of the claimed invention. Claims 8, 15, 23, 26, 28, 31-33 and 35-37 have been amended to more particularly define the invention.

It is noted that the claim amendments are made only for more particularly pointing out the invention, and not for distinguishing the invention over the prior art, narrowing the claims or for any statutory requirements of patentability. Further, Applicant specifically states that no amendment to any claim herein should be construed as a disclaimer of any interest in or right to an equivalent of any element or feature of the amended claim.

Claims 8, 15, 24-25, 27, 29-32 and 34-35 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795). Claim 26 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) and in further view of Shepard (US Patent No. 5,729,043). Claim 28 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) and in further view of Brewer (US Patent No. 6,322,600). Claims 23, 33 and 36-38 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Zheng (US Patent No. 5,728,621) in view of Liao (US Patent No. 6,110,795) as applied to claim 8 above, and further in view of Wolf ("Silicon Processing for The VLSI Era").

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a semiconductor substrate having a trench region comprising at least one trench, the trench comprising a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface, and a non-trench region having an upper surface which is substantially co-planar with the unpolished upper surface of the single layer of the HDP oxide.

Conventional substrates having shallow trench isolation (STI) regions require harsh

etching or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate. As a result the surface of the trench fill material includes scratches and chatter marks.

The claimed substrate, on the other hand, includes a trench region including at least one trench, the trench including a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface. Specifically, the claimed substrate includes a trench region having a doped HDP oxide which does not require a chemical mechanical polishing (CMP) step to be planarized with non-trench regions. Therefore, the doped HDP oxide may provide a low dielectric constant trench fill which does not necessarily include scratches and chatter marks.

II. THE PRIOR ART REFERENCES

A. The Zheng and Liao References

The Examiner alleges that Zheng would have been combined with Liao to form the claimed invention of claims 8, 15, 24-25, 27, 29-32 and 34-35. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Zheng discloses a method for forming planarized oxide shallow trench isolation. In the Zheng method, a high density plasma (HDP) oxide layer is deposited in the isolation trenches. A layer of spin-on-glass is coated over the HDP oxide layer. The spin-on-glass layer and portions of the HDP oxide layer remaining are polished away so that the substrate is planarized (Zheng at Abstract).

Liao discloses a method of correcting the scratches caused by CMP. In the Liao method, a microscratch formed in an isolation trench caused by chemical mechanical polishing is corrected by forming a sacrificial layer on the damaged trench fill so that the micro-scratch is thus filled with the sacrificial layer. Using a hard mask as an etch stop, the sacrificial layer is etched back. Since the etching rate of the sacrificial layer is the same as or lower than the isolation trench material, the formation of the micro-scratch is suppressed during the etching back process (Liao at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different problems. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), whereas Liao teaches a method of correcting the damage (e.g., microscratches) caused by CMP (Liao at col. 1, lines 13-17). Indeed, Zheng does not even recognize the surface damage (e.g., scratches, chatter marks) caused by CMP and, unlike Liao, does not take any action to correct the damage. Therefore, Liao specifically teaches that the Zheng device is defective. Clearly, these references teach away from each other so that no person of ordinary skill in the art would have considered combining the references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng by choosing a removal method taught by that will result in a substantially scratch free surface as taught by Liao with reasonable expectation of producing a trench fill with a planar surface with reduced surface flaws". However, the references do not include such a suggestion as alleged by the Examiner. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, contrary to the Examiner's allegations, neither Zheng nor Liao, nor any combination thereof, teaches or suggests "*a trench region comprising at least one trench, said trench comprising a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface*" as recited, for example, in claims 8, 15 and 23.

As noted above, conventional substrates having shallow trench isolation (STI) regions require harsh etching or chemical mechanical polishing (CMP) to planarize the surface of the substrate and filler material formed in trenches in the substrate (Application at page 2, lines 9-18). As a result the surface of the trench fill material includes scratches and chatter marks.

The claimed substrate, on the other hand, includes a trench region including at least one trench, the trench including a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface (Application at page 6, lines 2-3; Figure 7). Specifically,

the claimed substrate includes a doped HDP oxide which does not require a chemical mechanical polishing (CMP) step to be planarized non-trench regions. Therefore, the doped HDP oxide may provide a low dielectric constant trench fill which does not necessarily include scratches and chatter marks (Application at page 12, line 13-page 13, line 3).

Clearly, the cited references do not teach or suggest these novel features. Indeed, the Examiner expressly concedes that these references do not teach or suggest a doped HDP oxide in the trench region (e.g., see Office Action at page 4, lines 8-9).

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

B. The Shepard Reference

The Examiner alleges that Shepard would have been combined with Zheng and Liao to form the claimed invention of claim 26. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Shepard discloses a method of forming a shallow trench isolation (STI) using silicon dioxide. The STI includes a phosphorus layer formed below the surface of the deposited silicon dioxide layer (Shepard at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Shepard merely discloses a method of forming a phosphorus layer in a shallow trench isolation which is completely unrelated to Zheng and Liao. Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to substitute doped oxide for un-doped oxide ... to have an art-recognized equivalence". However, the

references do not include such a suggestion as alleged by the Examiner. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Zheng, nor Liao, nor Shepard, nor any combination thereof teaches or suggests "*a trench region comprising at least one trench, said trench comprising a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface*" as recited, for example, in claims 8, 15 and 23.

As noted above, unlike conventional substrates which use CMP to planarize the surface of the substrate and filler material, the claimed substrate includes at least one trench including a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface (Application at page 6, lines 2-3; Figure 7). Specifically, the doped HDP oxide does not require a chemical mechanical polishing (CMP) step to be planarized non-trench regions. Therefore, the doped HDP oxide may provide a low dielectric constant trench fill which does not necessarily include scratches and chatter marks (Application at page 12, line 13-page 13, line 3).

Clearly, these features are not taught or suggested by Shepard. Indeed, Shepard does not even mention a problem (e.g., scratches and chatter marks on trench fill material) which the claimed invention was intended to address.

Further, the Examiner relies on the passage at column 4, lines 46-47 of Shepard to support his position. However, this passage merely discloses an SiO_2 layer having phosphorus implanted therein. That is, the passage does not teach or suggest a doped HDP oxide. In fact, nowhere does Shepard recognize an importance of using a HDP oxide as a trench fill material.

Applicant respectfully submits that doped silicon oxide layer is not necessarily the same as a doped HDP oxide layer. Indeed, as explained in the Application, HDP oxide provides desirable qualities for formation of a trench region which are not trivial.

Moreover, the reason that Shepard gives for forming phosphorus in the STI is "to tie up any sodium ionic contamination from processes prior to gate formation". Clearly, this is

completely unrelated to any purpose of the claimed invention. Therefore, contrary to the Examiner's allegations, Shepard does not make up for the deficiencies of Zheng and Liao.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

C. The Brewer Reference

The Examiner alleges that Brewer would have been combined with Zheng and Liao to form the claimed invention of claim 28. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Brewer discloses a planarization composition for chemical mechanical planarization of dielectric layers for semiconductor manufacture, and methods for using the planarization composition in the manufacture of semiconductor devices (Brewer at Abstract).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), and Liao teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), whereas Brewer is merely directed to a planarization composition for CMP (Brewer at col. 1, lines 13-17). Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng and Liao by adding dopant to the oxide trench fill as suggested by Brewer to produce a trench fill of a desired dielectric constant". However, the references do not include such a suggestion as alleged by the Examiner. Therefore, Applicant respectfully submits that one of

ordinary skill in the art would not have been so motivated to combine the references as alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Zheng, nor Liao, nor Brewer, nor any combination thereof teaches or suggests "*a trench region comprising at least one trench, said trench comprising a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface*" as recited, for example, in claims 8, 15 and 23.

As noted above, unlike conventional substrates which use CMP to planarize the surface of the substrate and filler material, the claimed substrate includes at least one trench including a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface (Application at page 6, lines 2-3; Figure 7). Specifically, the doped HDP oxide does not require a chemical mechanical polishing (CMP) step to be planarized non-trench regions. Therefore, the doped HDP oxide may provide a low dielectric constant trench fill which does not necessarily include scratches and chatter marks (Application at page 12, line 13-page 13, line 3).

Clearly, these features are not taught or suggested by Brewer. Indeed, Brewer does not even mention a problem (e.g., scratches and chatter marks on trench fill material) which the claimed invention was intended to address.

The Examiner alleges that Brewer teaches filling a trench with a dielectric that includes boron doped oxide glass or phosphorus doped oxide glass "and HDP oxides". That is, the Examiner concedes that Brewer does not teach or suggest doped HDP oxide as a trench fill material.

Further, Brewer is merely directed to a composition for chemical mechanical polishing and is unrelated to the claimed substrate. Brewer may disclose a trench region in a substrate (Brewer at Figure 7b). However, the whole point of Brewer is to improve a CMP process for forming a trench region (Brewer at col. 11, line 40- col. 12, line 22). Applicant notes that it is very unlikely that any person of ordinary skill in the art would rely upon Brewer whose primary objective is to improve a CMP process, to form the claimed invention having an important objective of eliminating a processing (e.g., etching and CMP) of the

HDP oxide in the trench.

Clearly, Brewer does not teach or suggest a trench including a doped HDP oxide. Therefore, contrary to the Examiner's allegations, Brewer does not make up for the deficiencies of the other references.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

D. The Wolf Reference

The Examiner alleges that Wolf would have been combined with Zheng and Liao to form the claimed invention of claims 23, 33 and 36-38. Applicant submits, however, that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention.

Wolf discloses a boron-doped trench filler material (Wolf at page 48).

However, Applicant submits that these references would not have been combined as alleged by the Examiner. Indeed, these references are directed to different matters. Specifically, Zheng planarizes a substrate surface by chemical mechanical polishing (CMP), and Liao teaches that CMP damages a substrate surface and planarizing the substrate surface by filling the damaged areas (e.g., microscratches) (Laio at col. 1, lines 13-17), whereas Wolf is merely directed to a boron-doped trench fill. Therefore, no person of ordinary skill in the art would have considered combining these references.

Further, Applicant submits that the Examiner can point to no motivation or suggestion in the references to urge the combination as alleged by the Examiner. Indeed, the Examiner supports the combination by merely stating that it would have been obvious "to modify Zheng and Liao by having dopants such as boron as taught by Wolf to be conventional practice, to produce an isolation trench that separates devices". However, the references do not include such a suggestion as alleged by the Examiner. Therefore, Applicant respectfully submits that one of ordinary skill in the art would not have been so motivated to combine the references as

alleged by the Examiner. Therefore, the Examiner has failed to make a prima facie case of obviousness.

Moreover, neither Zheng, nor Liao, nor Wolf, nor any combination thereof teaches or suggests "*a trench region comprising at least one trench, said trench comprising a single layer of doped high-density plasma (HDP) oxide having an unpolished upper surface*" as recited, for example, in claims 8, 15 and 23.

As noted above, in the claimed substrate, the doped HDP oxide does not require a chemical mechanical polishing (CMP) step to be planarized non-trench regions. Therefore, the doped HDP oxide may provide a low dielectric constant trench fill which does not necessarily include scratches and chatter marks (Application at page 12, line 13-page 13, line 3).

Clearly, these features are not taught or suggested by Wolf. Indeed, Wolf does not even mention a problem (e.g., scratches and chatter marks on trench fill material) which the claimed invention was intended to address.

Further, Applicant notes that Wolf is merely cited by the Examiner as allegedly teaching implanting dopants in a non-trench region. The Examiner attempts to rely on pages 48 and 522-523 to support his allegations. However, nowhere do these passages teach or suggest a trench including an HDP oxide let alone a doped HDP oxide. Therefore, contrary to the Examiner's allegations, Wolf does not make up for the deficiencies of the other references.

Therefore, Applicant submits that these references would not have been combined and even if combined, the combination would not teach or suggest each and every element of the claimed invention. Therefore, the Examiner is respectfully requested to withdraw this rejection.

III. FORMAL MATTERS AND CONCLUSION

In view of the foregoing, Applicant submits that claims 8, 15 and 23-38, all the claims presently pending in the application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above

RECEIVED
CENTRAL FAX CENTER
OCT 22 2003

OFFICIAL

application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 09-0456.

Respectfully Submitted,

Date: 10/21/03

Phillip E. Miller
Reg. No. 46,060

McGinn & Gibb, PLLC
8321 Old Courthouse Road, Suite 200
Vienna, VA 22182-3817
(703) 761-4100
Customer No. 21254

CERTIFICATE OF FACSIMILE TRANSMISSION

I hereby certify that the foregoing Amendment was filed by facsimile with the United States Patent and Trademark Office, Examiner David Blum, Group Art Unit # 2813 at fax number (703) 872-9318 this 21st day of October, 2003.

Phillip E. Miller
Reg. No. 46,060

IN THE CLAIMS:

8. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising at least one trench, said trench comprising a single layer of ~~seamless~~ doped high-density plasma (HDP) ~~HDP~~ oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said ~~seamless~~ HDP oxide,

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.~~

15. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising a plurality of trenches, each of said trenches comprising a single layer of doped ~~seamless~~ high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants; ~~and~~

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back.~~

23. (Currently Amended) A semiconductor substrate comprising:

a trench region comprising at least one wide trench and at least one narrow trench ~~a plurality of trenches~~, each of said trenches comprising a single layer of doped ~~seamless~~ high density plasma (HDP) oxide having an unpolished upper surface; and

a non-trench region having an upper surface which is substantially co-planar with said unpolished upper surface of said single layer of said seamless HDP oxide,

wherein said upper surface of said non-trench region comprises implanted dopants; ~~and~~

~~wherein said upper surface of said HDP oxide and said upper surface of said non-trench region are planarized without etch-back~~.

24. (Previously presented) The semiconductor substrate according to claim 8, wherein said high density plasma oxide comprises non-conformal high density plasma oxide.

25. (Previously presented) The semiconductor substrate according to claim 8, wherein said at least one trench comprises at least one wide trench and at least one narrow trench.

26. (Currently amended) The semiconductor substrate according to claim 8, wherein said doped high density plasma oxide comprises fluorine-doped high density plasma oxide ~~a low dielectric constant oxide~~.

27. (Previously presented) The semiconductor substrate according to claim 1, wherein said high density plasma oxide comprises silicon dioxide.

28. (Currently amended) The semiconductor substrate according to claim 24, wherein said high density plasma oxide comprises silicon dioxide doped with ~~one of phosphorus, boron and~~ fluorine.

29. (Previously presented) The semiconductor substrate according to claim 8, wherein said surface of said filler material and said surface of said substrate are planarized without reactive ion etching.

30. (Previously presented) The semiconductor substrate according to claim 8, wherein said at least one trench comprises shallow trench isolations.

31. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide and said upper surface of said non-trench region are planarized without chemical mechanical polishing.

32. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide is substantially scratch-free.

33. (Currently amended) The semiconductor substrate according to claim 8, wherein said surface of said non-trench region ~~substrate~~ comprises implanted dopants.

34. (Previously presented) The semiconductor substrate according to claim 8, further comprising:

a thin oxide layer grown on said upper surface of said substrate.

35. (Currently amended) The semiconductor substrate according to claim 8, wherein said upper surface of said single layer of ~~seamless~~ HDP oxide is free of chatter marks.

36. (Currently amended) The semiconductor substrate according to claim 23, wherein said ~~at least one trench comprises~~ at least one wide trench is formed adjacent to said ~~and~~ at least one narrow trench.

37. (Currently amended) The semiconductor substrate according to claim 23, wherein said doped HDP oxide comprises fluorine-doped HDP oxide ~~implanted dopants comprise at least one of phosphorus, boron and fluorine~~.

38. (Previously presented) The semiconductor substrate according to claim 23, wherein said high density plasma (HDP) oxide comprises non-conformal HDP oxide.

39. (New) The semiconductor substrate according to claim 37, further

comprising:

G1

a thin oxide layer grown on said upper surface of said substrate, said thin oxide layer comprises a high-purity oxide.

40. (New) The semiconductor substrate according to claim 8, wherein a thickness of said single layer of HDP oxide comprises an as-deposited thickness.